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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,826	04/13/2000	David E. Charlton	4076US(99-01860)	7750

7590 10/19/2005

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,826	CHARLTON ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.1 14, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on August 30, 2005 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-19 rejected under 35 U.S.C. 102(e) as being anticipated by Dell et al. U.S. Patent No. 5,996,096.

As per claim 1, Dell et al. teach the claimed memory module (SIMM) having a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate; and at least one discrete non-volatile storage device (EPROM) disposed on the memory module carrier substrate (column 2 lines 51-64), the discrete non-volatile storage device configured for storing data indicating a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location) .

As per claim 2, Dell et al. teach that the memory module uses a non-volatile storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52).

As per claim 3, Dell et al. teach the memory module contains at least one failed output (column 3 lines 7-35).

As per claim 4, Dell et al. teach the memory module in which a portion of the plurality of discrete memory devices are fully functional dice (Figure 9 A-B, column 6 lines 9-16). The examiner interprets the term 'fully functional dice' in the memory

industry as one in which all 'bad' cells can be remapped or blocked from use.

As per claim 5, Dell et al. teach a computer system, having a processor (ASIC) and a memory module (SIMM) with a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate and at least one discrete non-volatile storage device (EPROM) disposed on the memory module carrier substrate (column 2 lines 51-64), the at least one discrete non-volatile storage device configured for storing data indicating a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location) .

As per claim 6, Dell et al. teach that the memory module uses a non-volatile storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52).

As per claim 7, Dell et al. teach the memory module contains at least one failed output (column 3 lines 7-35).

As per claim 8, Dell et al. teach the memory module in which a portion of the plurality of discrete memory devices are fully functional dice (Figure 9 A-B, column 6

lines 9-16). The examiner interprets the term 'fully functional dice' in the memory industry as one in which all 'bad' cells can be remapped or blocked from use.

As per claim 9, Dell et al teach the testing of a memory module (Figure 9A-E). The memory module (SIMM) with a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate and identifying data indicative of a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 6 lines 19-21); and storing the identified data (column 6 lines 21-24) on the memory module (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location) .

As per claim 10, Dell et al. teach storing the identification of at least one failed output (column 3 lines 7-35, column 6 lines 21-24, figure 9C-D).

As per claim 11, Dell et al teach storing the identification of the failed output in the discrete non-volatile storage device on the memory module (column 6 lines 19-24 Figure 9C-D).

As per claim 12, Dell et el. teach that the memory module uses a non-volatile storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52, column 6 lines 19-24 Figure 9C-D).

As per claim 13, Dell et al. teach accessing the stored data and identifying the location of the at least one of the plurality of discrete memory devices associated with the at least one refurbishable failure (Figure 9D-E column 6 lines 31-36).

As per claim 14, Dell et al. teaches repairing or replacing discrete memory devices on the memory module carrier substrate identified as having the at least one refurbishable failure (Figure 9E column 6 lines 40-49).

As per claim 15, Dell et al teach a method of fabricating a memory module (SIMM) by placing a plurality of discrete memory devices (DRAM) on a memory module carrier substrate (printed circuit board), testing each of a plurality of elements associated with each of the plurality of discrete memory devices on the memory module carrier substrate and storing data indicative of a location of at least one discrete memory device including at least one element which failed a test. (Figures 9A-E column 6 lines 11-49)

As per claim 16, Dell et al. teach accessing the stored data indicative of the location of the at least one discrete memory device including the at least one element which failed the test (Figure 9D-E column 6 lines 31-36).

As per claim 17, Dell et al. teach identifying the at least one discrete memory

device having the at least one failed element and repairing or replacing the at least one identified discrete memory device on the memory module substrate (Figure 9E column 6 lines 40-49).

As per claim 18, Dell et al teach testing the repaired or replaced discrete memory device on the memory module substrate (Figure 9E, column 6 lines 36-52).

As per claim 19, Dell et al. teach storing the data indicative of the location (by bit, row, column or by chip ID) of the discrete memory device including the at least one element which failed the test including storing data indicative of at least one failed output (Figure 9C-E column 6 lines 19-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133